



# INVESTOR MEETING 2014

William Holt

Executive Vice President  
General Manager, Technology and Manufacturing Group

# Key Messages from 2013

Intel Continues to Deliver the Benefits of Moore's Law



True Cost Reduction Remains Possible in a Capital Intensive Environment



The Benefits of Technology Apply Across the Product Portfolio

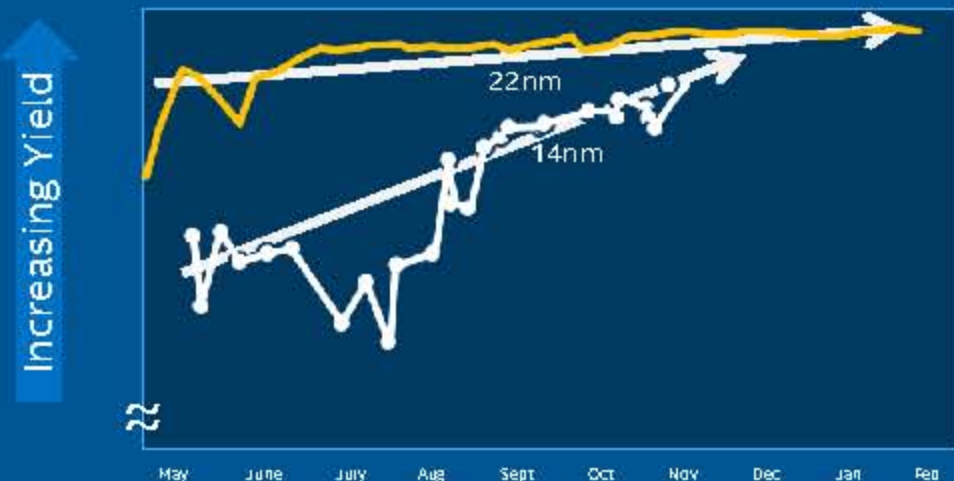




# 14nm Status - 2013

## Yield

at the same point in development



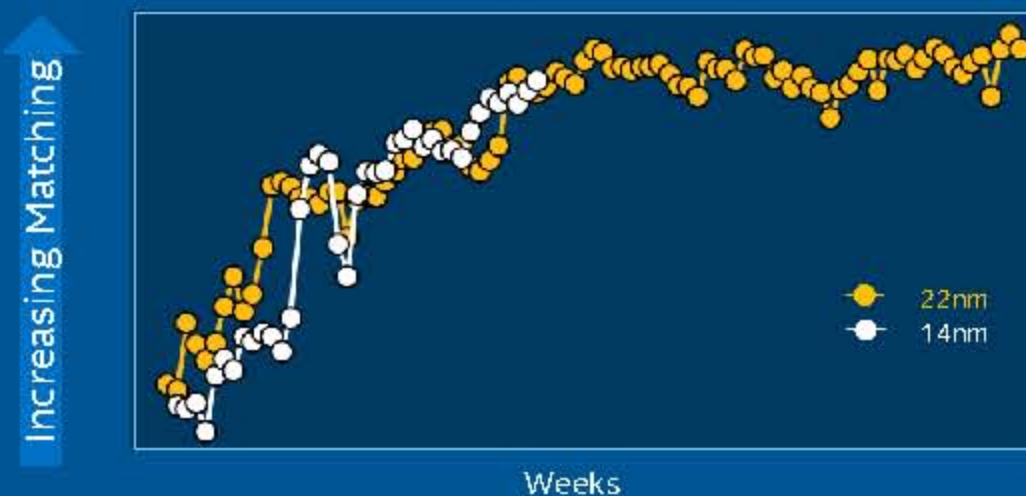
## Performance Improvement

Switching Energy vs. Gate Delay



## Key Parameter Matching

% of key process parameters meeting 3-sigma targets at the same point in development



## Reliability Scorecard

at the same point in development

Module	22nm (2 year offset)	14nm	
Transistor	Low risk	Low risk	Low risk Meeting all cert goals
Interconnect	Low risk	Low risk	Low risk Meeting all cert goals
Thermo-Mechanical/Moisture	High risk	Low risk	Medium risk Close to meeting goals
Test Vehicle Yield	Medium risk	High risk	High risk Not yet meeting all goals, needs additional work
ESD/LU	Low risk	Low risk	Low risk Meeting all cert goals
Alpha Particle/Soft Error	Medium risk	Low risk	Medium risk Close to meeting goals

Generally healthy reliability at this stage, on track for Q1 '14 certification \*

# 14nm Status - 2014

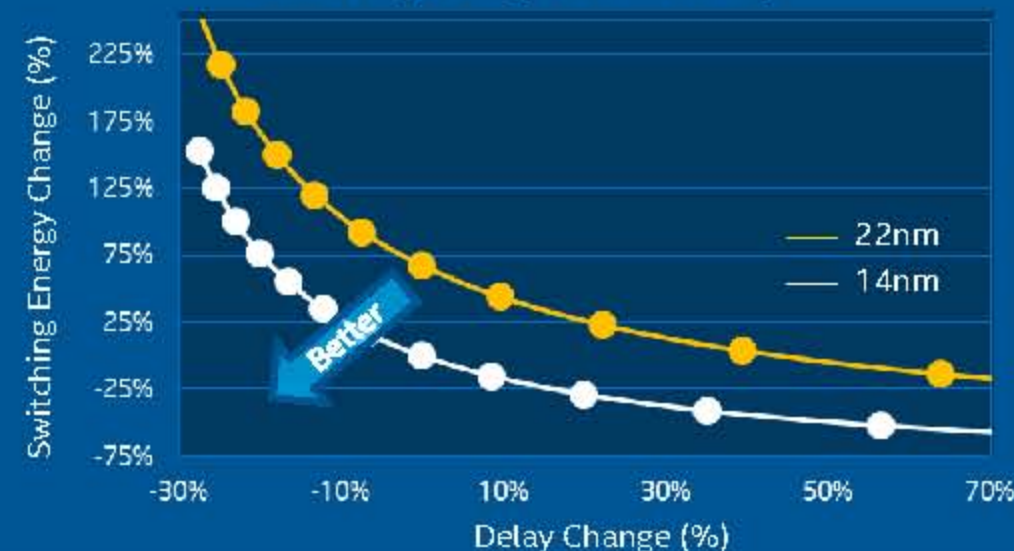
## Yield

at the same point in development



## Performance Improvement

Switching Energy vs. Gate Delay



## Key Parameter Matching

% of key process parameters meeting 3-sigma targets  
at the same point in development



14 nm key process parameter matching on track with 22 nm trend

## Reliability Scorecard

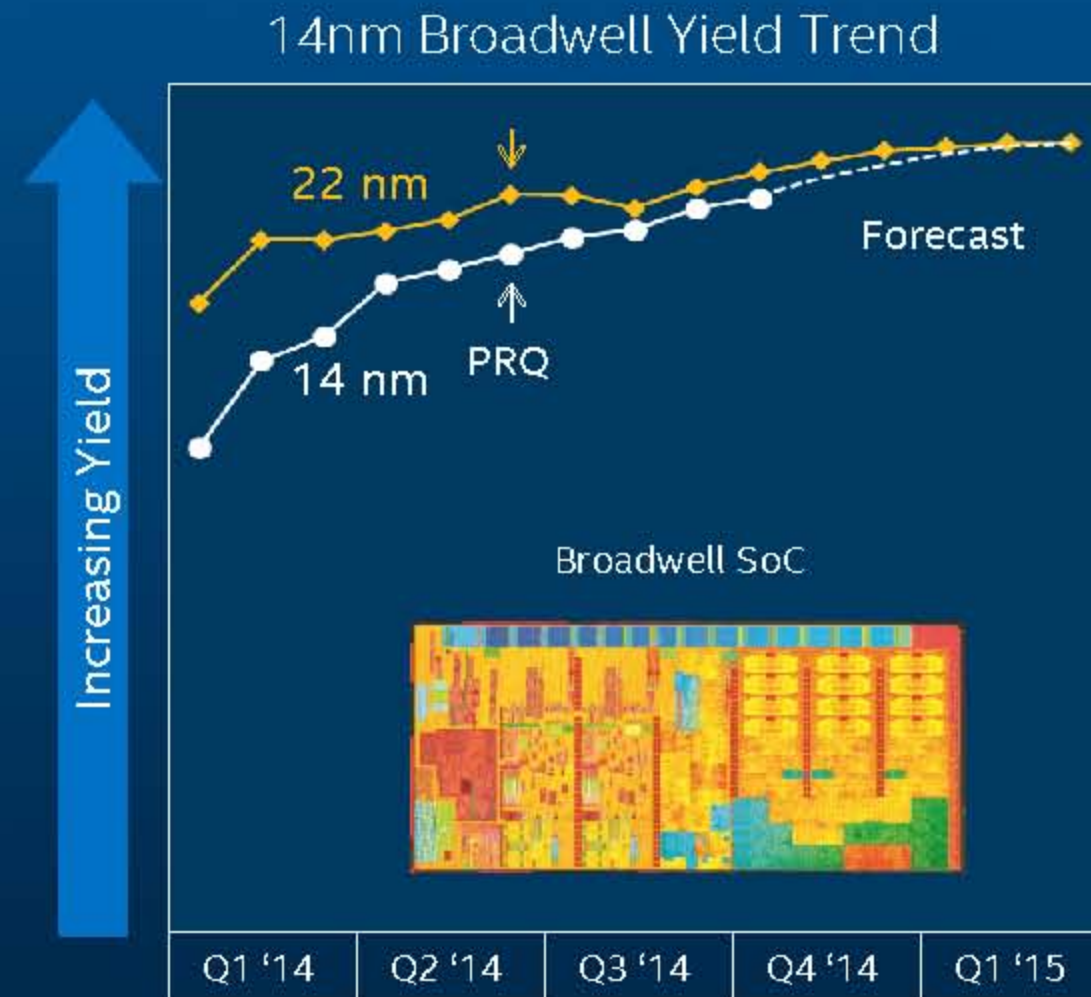
at the same point in development

Module	22nm (2 year offset)	14nm
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Alpha Particle/Soft Error	Low risk	Low risk

14nm PRQ achieved Q2 2014



# 14 nm Product Yield Is In Healthy Range



22 nm data are shifted to align date of lead product qual  
Depicts relative health, lines not to scale

## 22nm Is Intel's Highest Yielding Process Ever

# 14nm Technology Overview

A True 14 nm Technology

2nd Generation FinFET

52 nm Interconnect Pitch

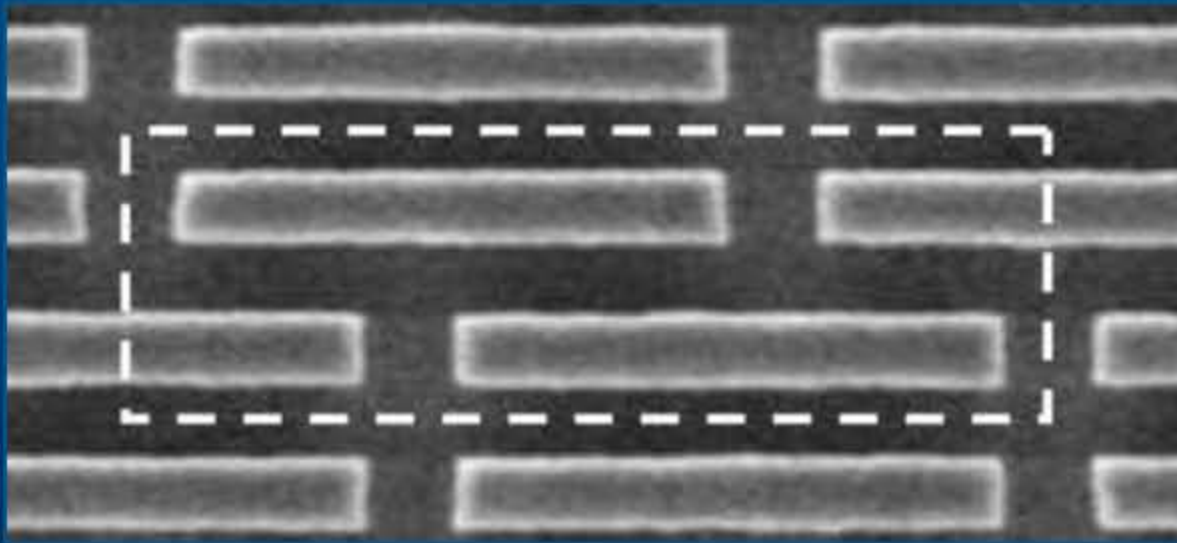
First Use of Air Gaps

# Intel Has Developed a True 14 nm Technology

	22 nm Node	14 nm Node	Scale
Transistor Fin Pitch	60	42	.70x
Transistor Gate Pitch	90	70	.78x
Interconnect Pitch	80 nm	52 nm	.65x

# SRAM Memory Cells

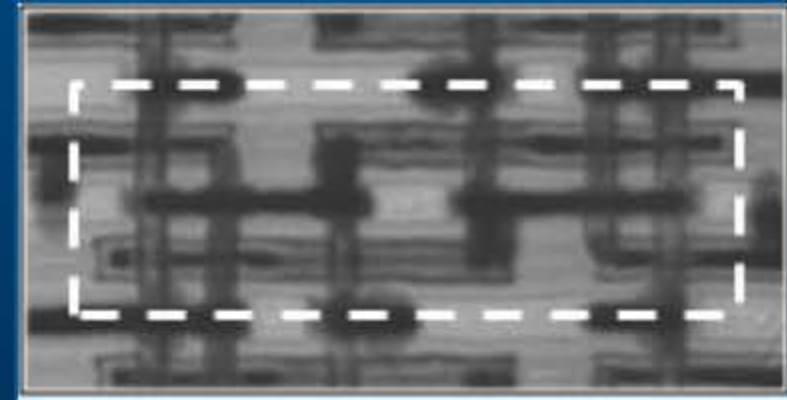
22 nm Process



.108  $\mu\text{m}^2$

(Used on CPU products)

14 nm Process



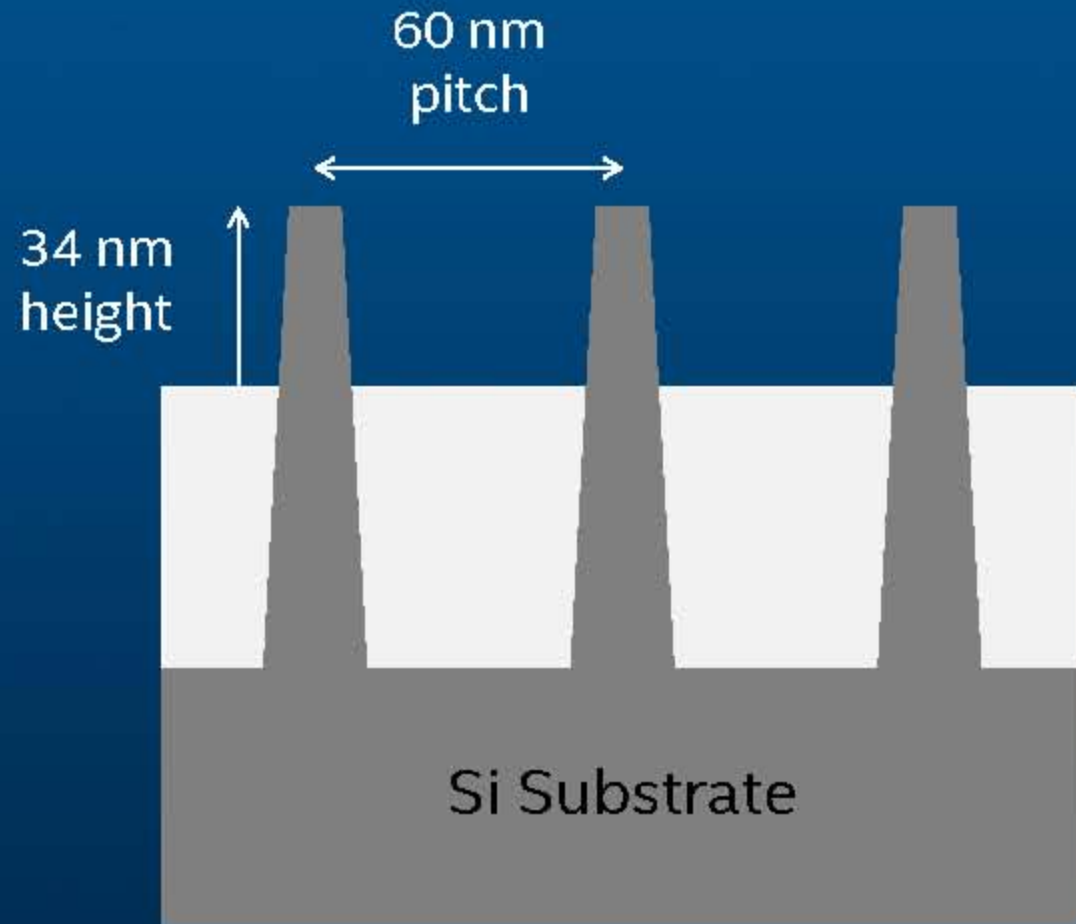
.0588  $\mu\text{m}^2$

(0.54x area scaling)

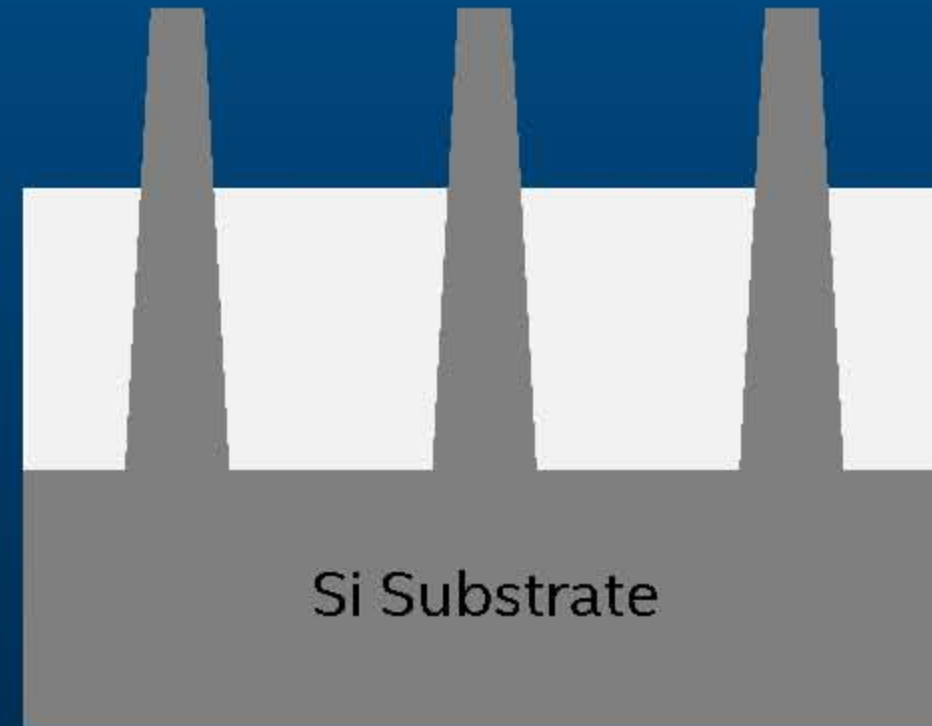
***14 nm Design Rules + 2<sup>nd</sup> Generation Tri-gate Transistor Provides Industry-leading SRAM Density***



# Transistor Fin Improvement

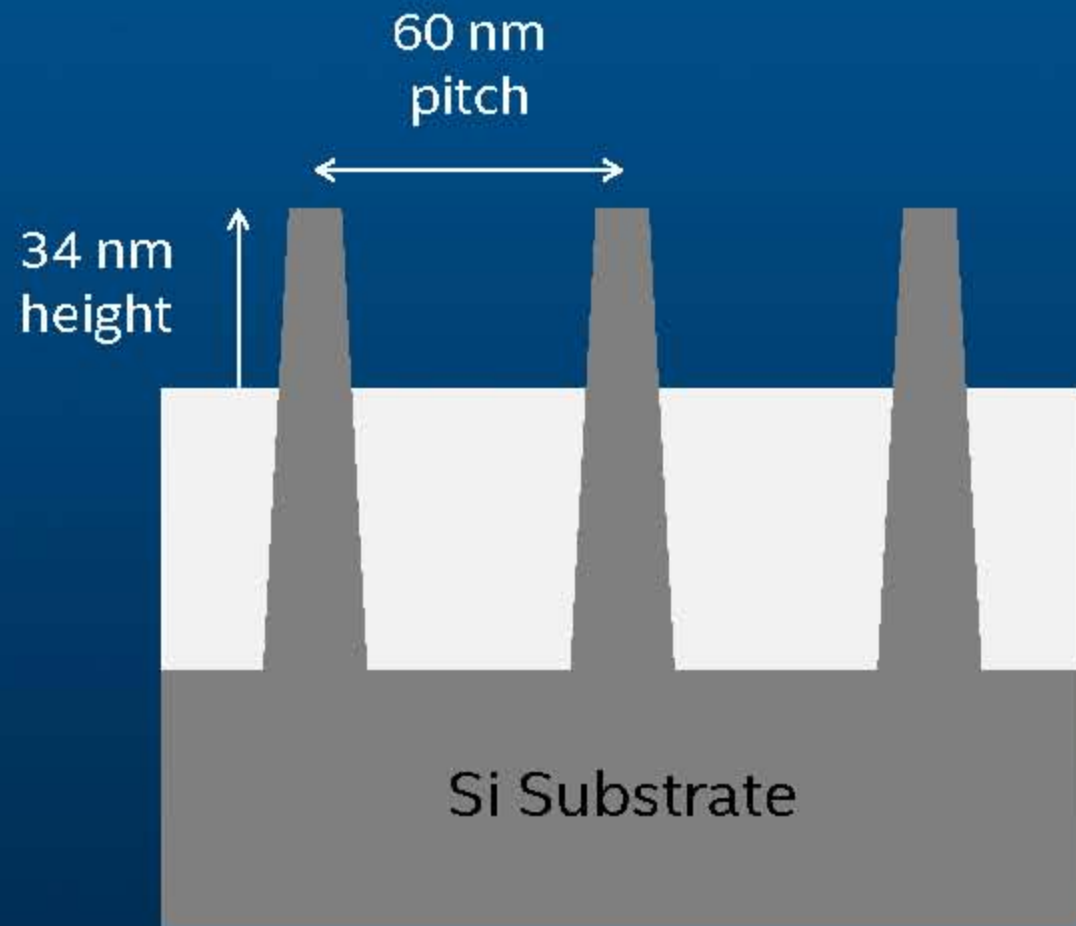


22 nm Process

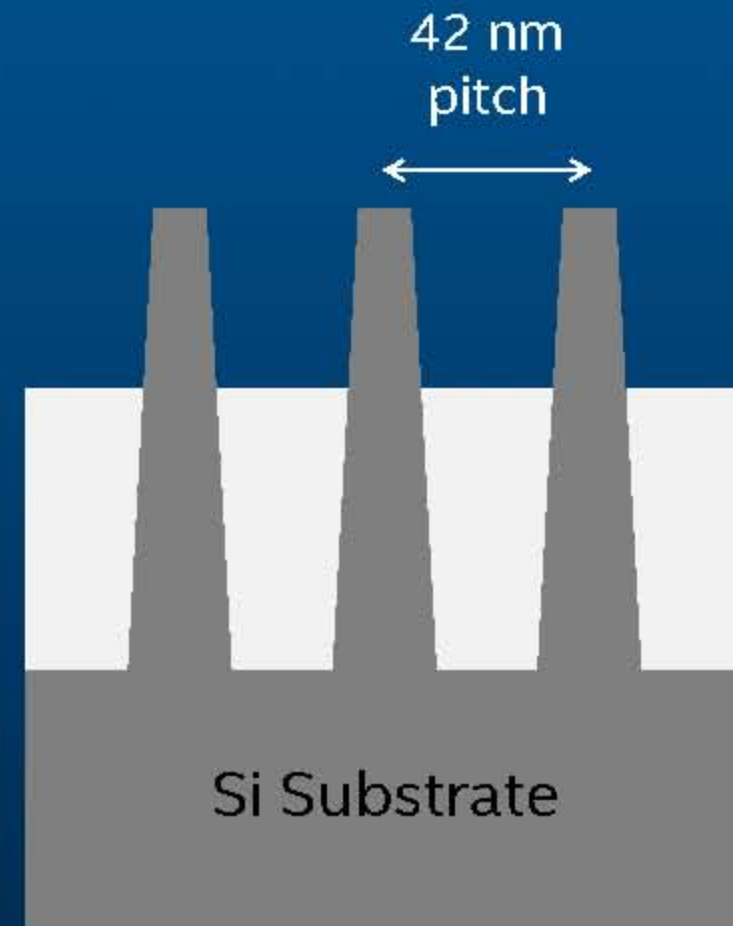


14 nm Process

# Transistor Fin Improvement



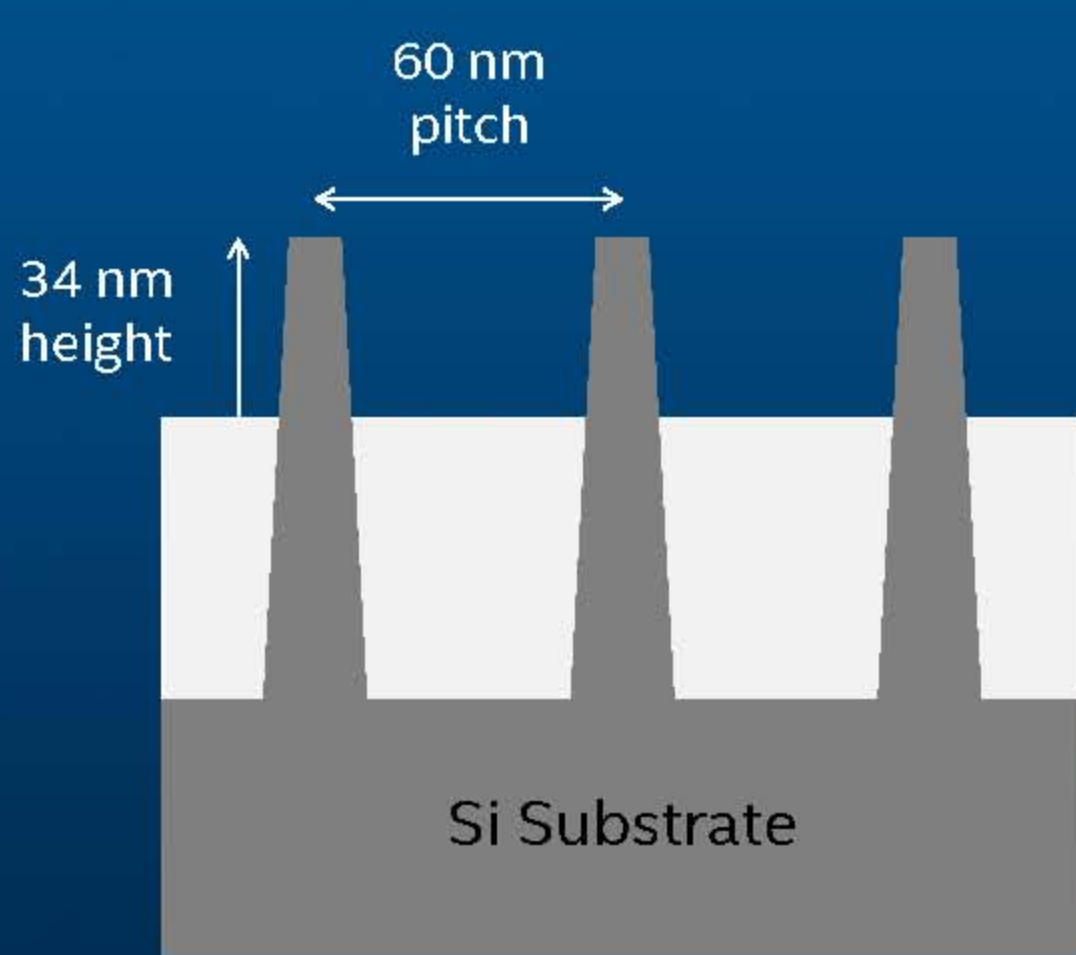
22 nm Process



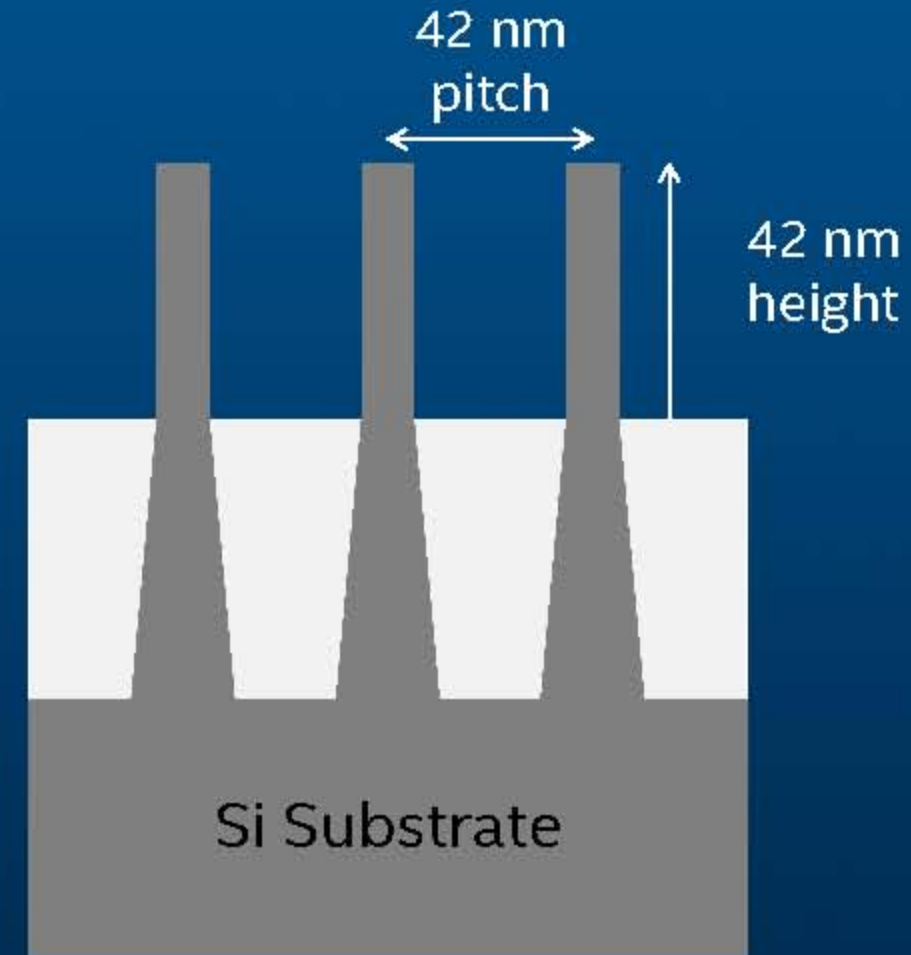
14 nm Process

***Tighter Fin Pitch for Improved Density***

# Transistor Fin Improvement



22 nm Process

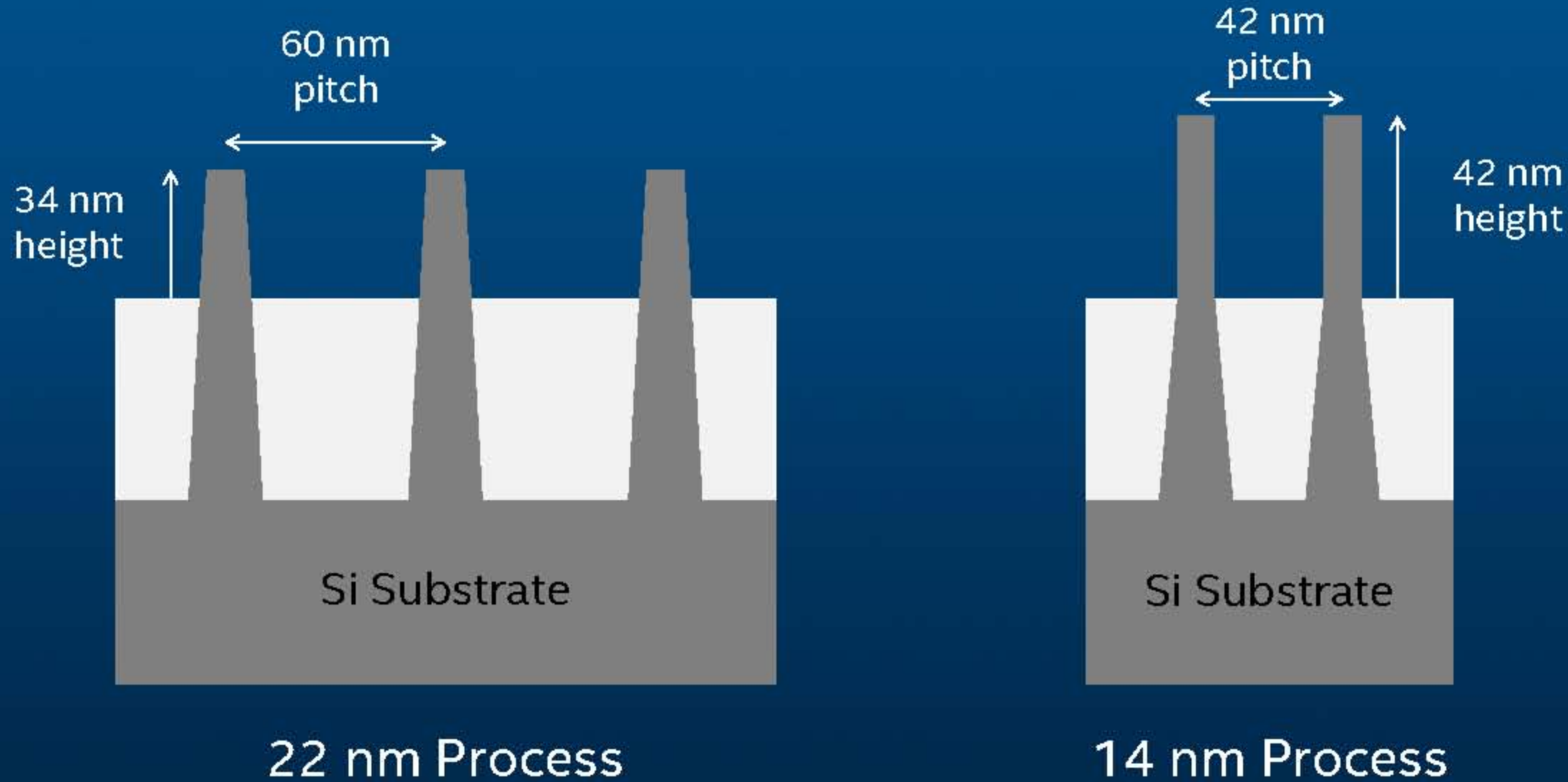


14 nm Process

***Taller and Thinner Fins for Increased Drive Current and Performance***

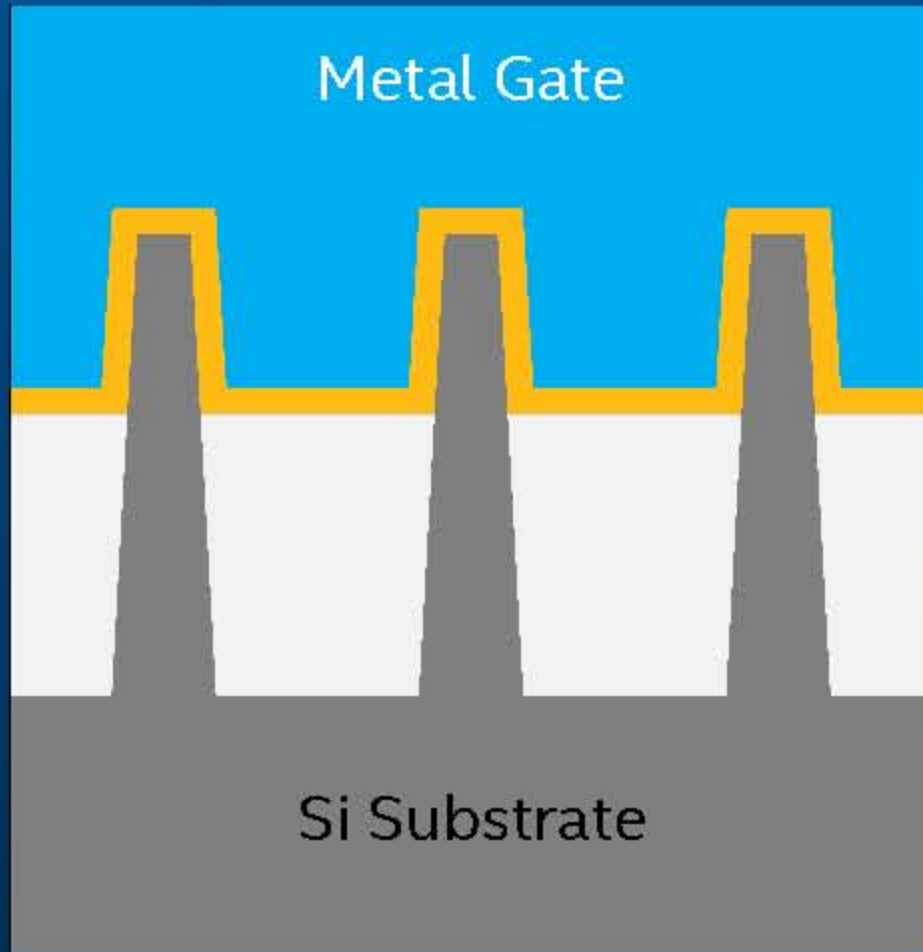


# Transistor Fin Improvement



***Reduced Number of Fins for Improved Density  
and Lower Capacitance***

# Transistor Fin Improvement

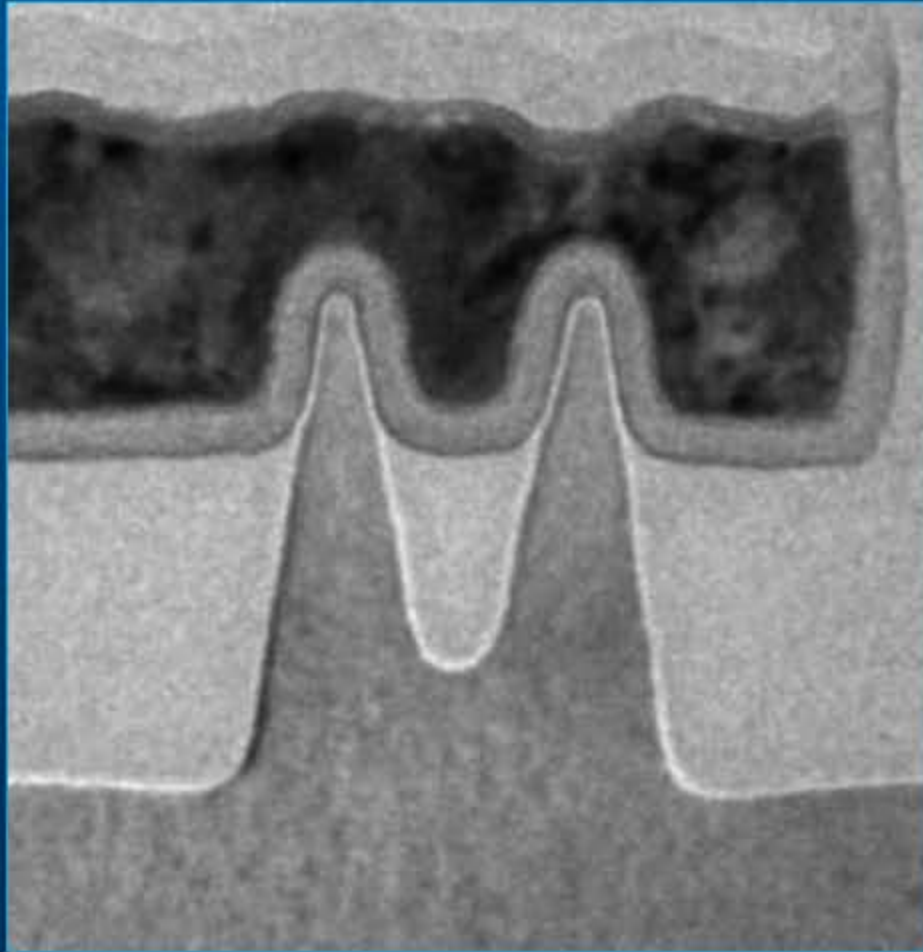


22 nm 1<sup>st</sup> Generation  
Tri-gate Transistor

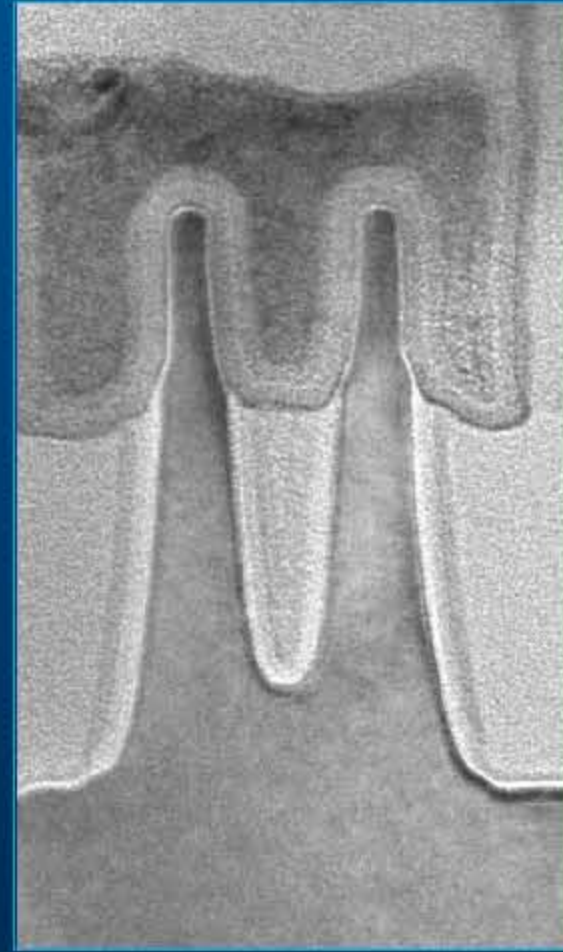


14 nm 2<sup>nd</sup> Generation  
Tri-gate Transistor

# Transistor Fin Improvement



22 nm 1<sup>st</sup> Generation  
Tri-gate Transistor



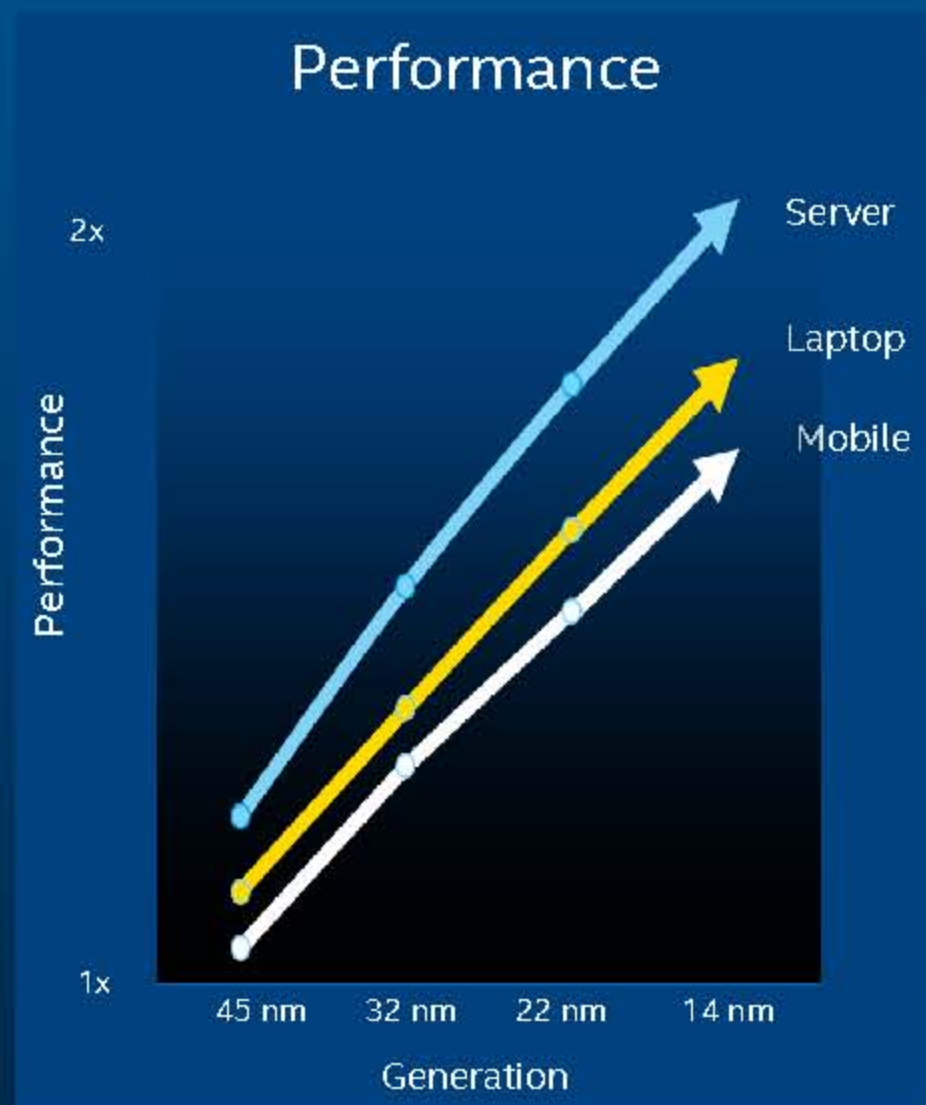
14 nm 2<sup>nd</sup> Generation  
Tri-gate Transistor



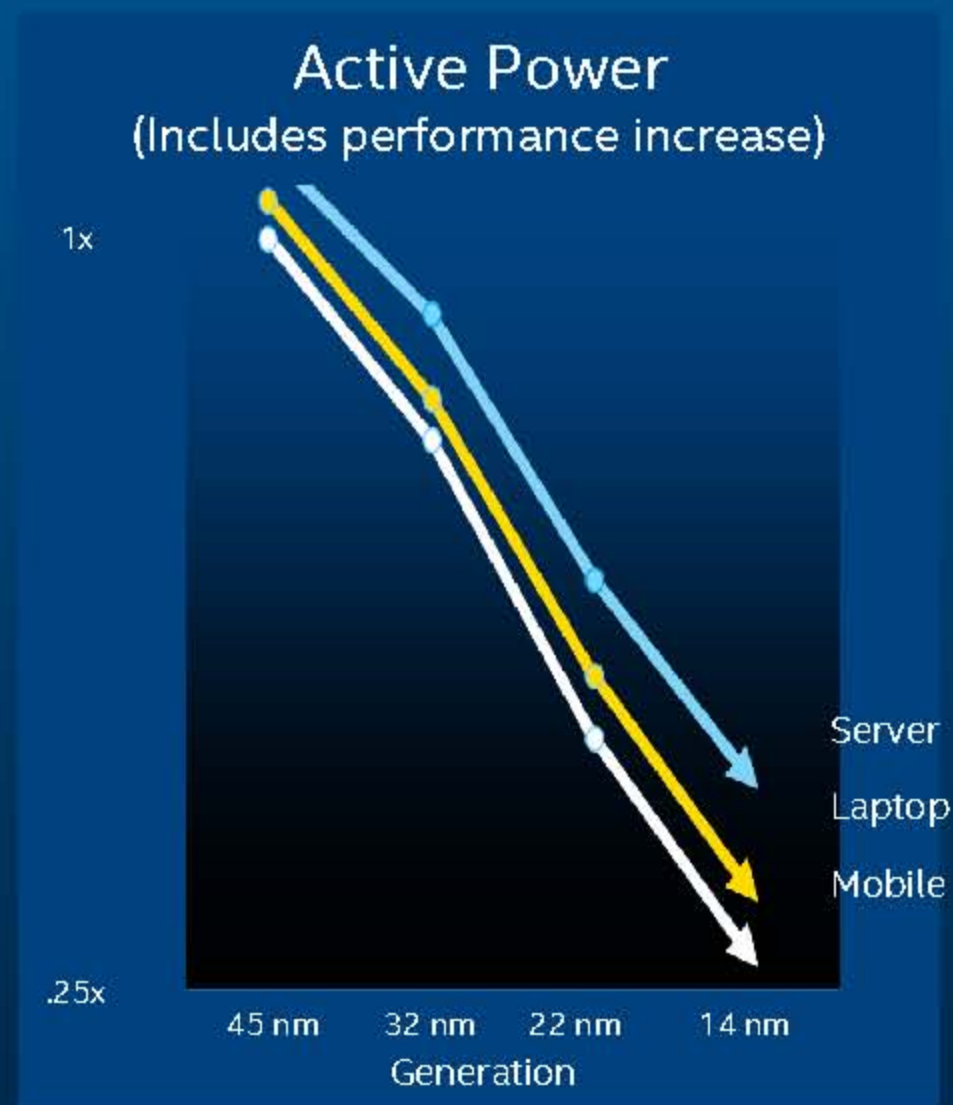
# Intel Transistor Leadership



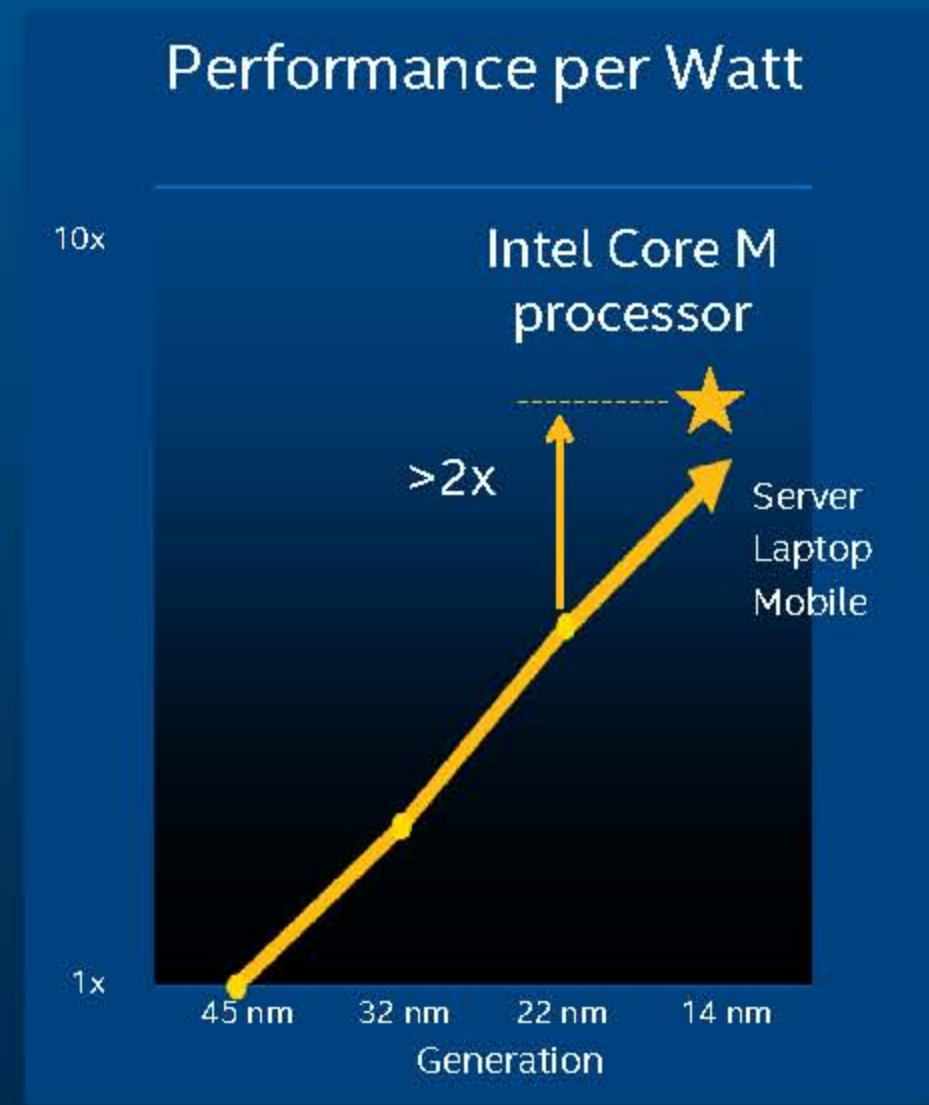
# 2<sup>nd</sup> Generation Tri-Gate is the Critical Enabler



*Performance Improved*



*Active Power Reduced*



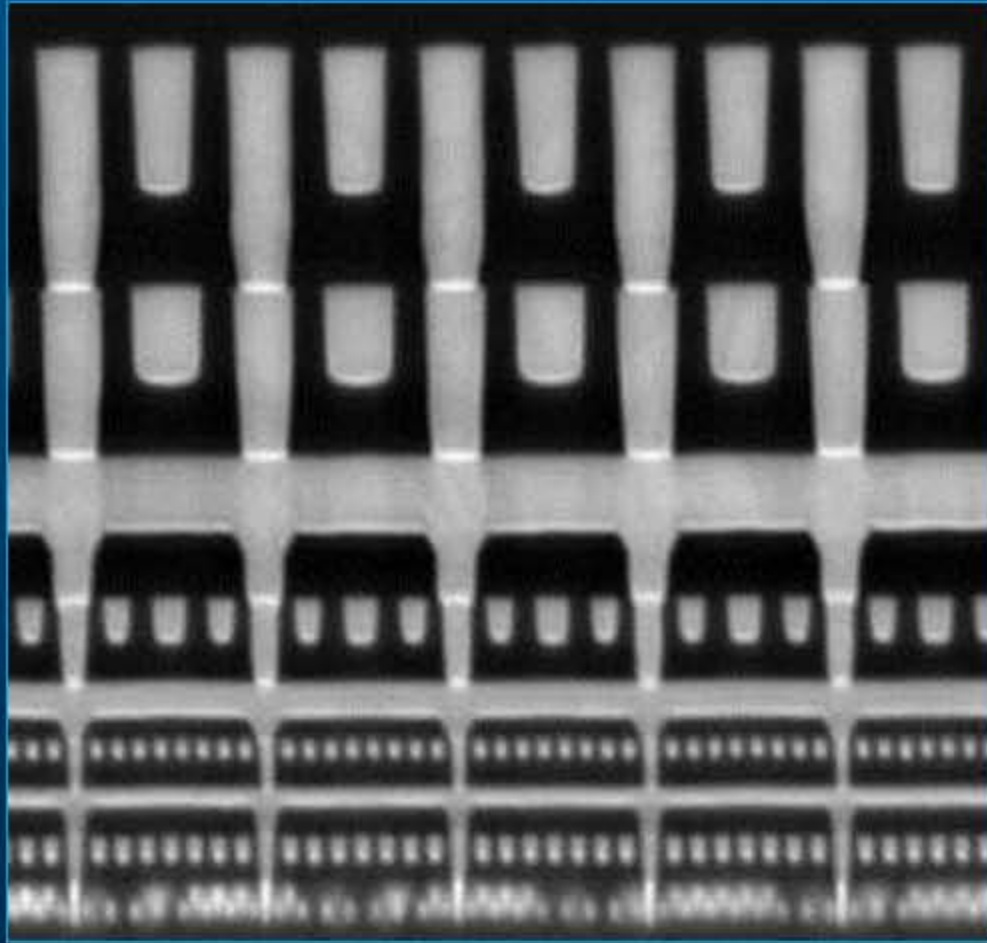
*Performance per Watt Improves*

**14 nm BDW-Y Delivers >2x Improvement in Performance per Watt**



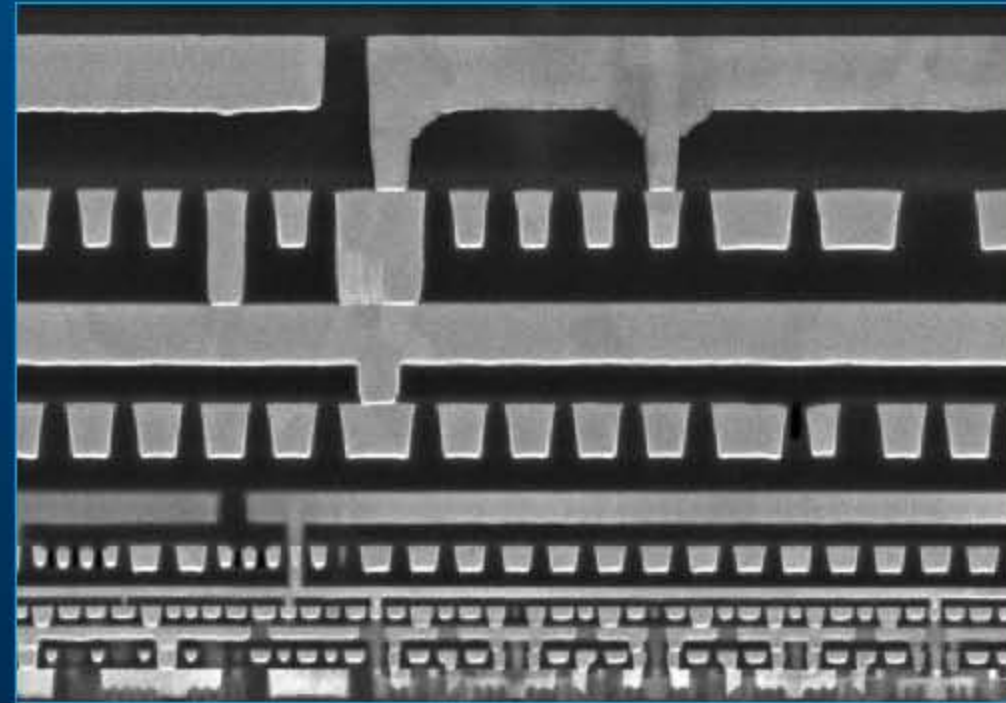
# Interconnects

22 nm Process



80 nm minimum pitch

14 nm Process



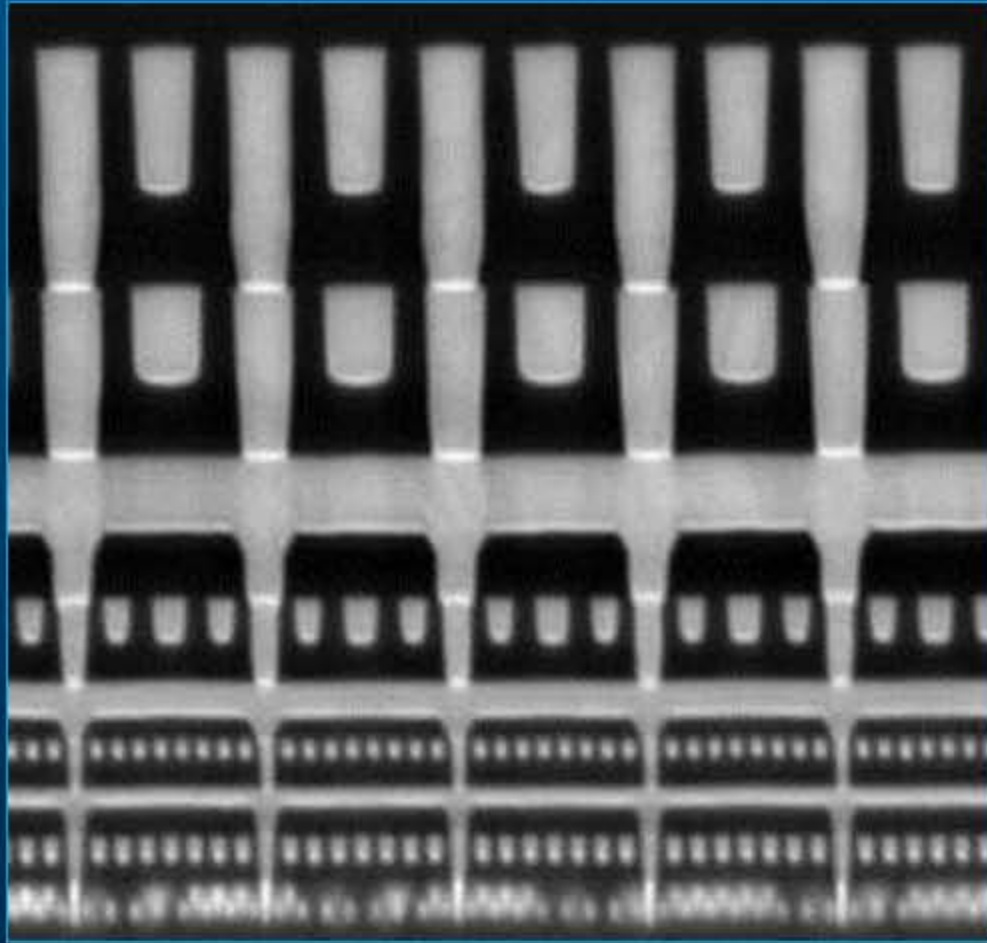
52 nm (0.65x) minimum pitch

***52 nm Interconnect Pitch Provides Better-than-normal Interconnect Scaling***



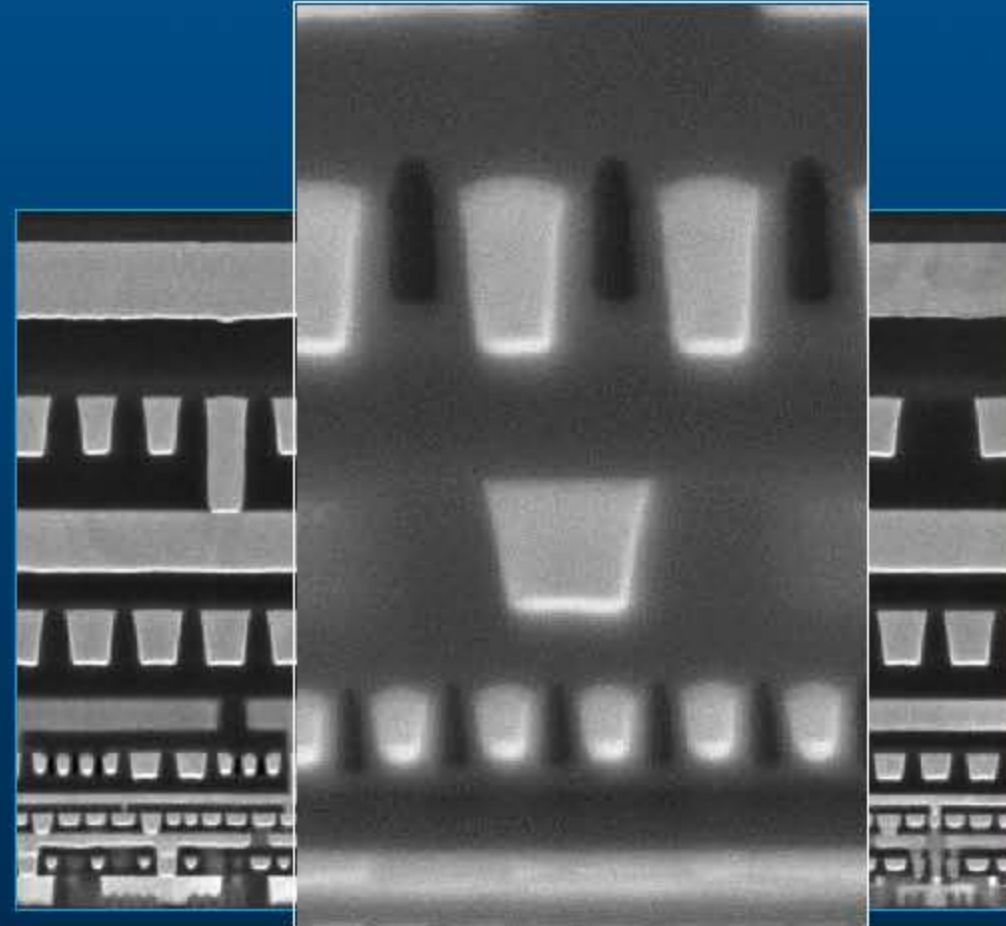
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14 nm Process

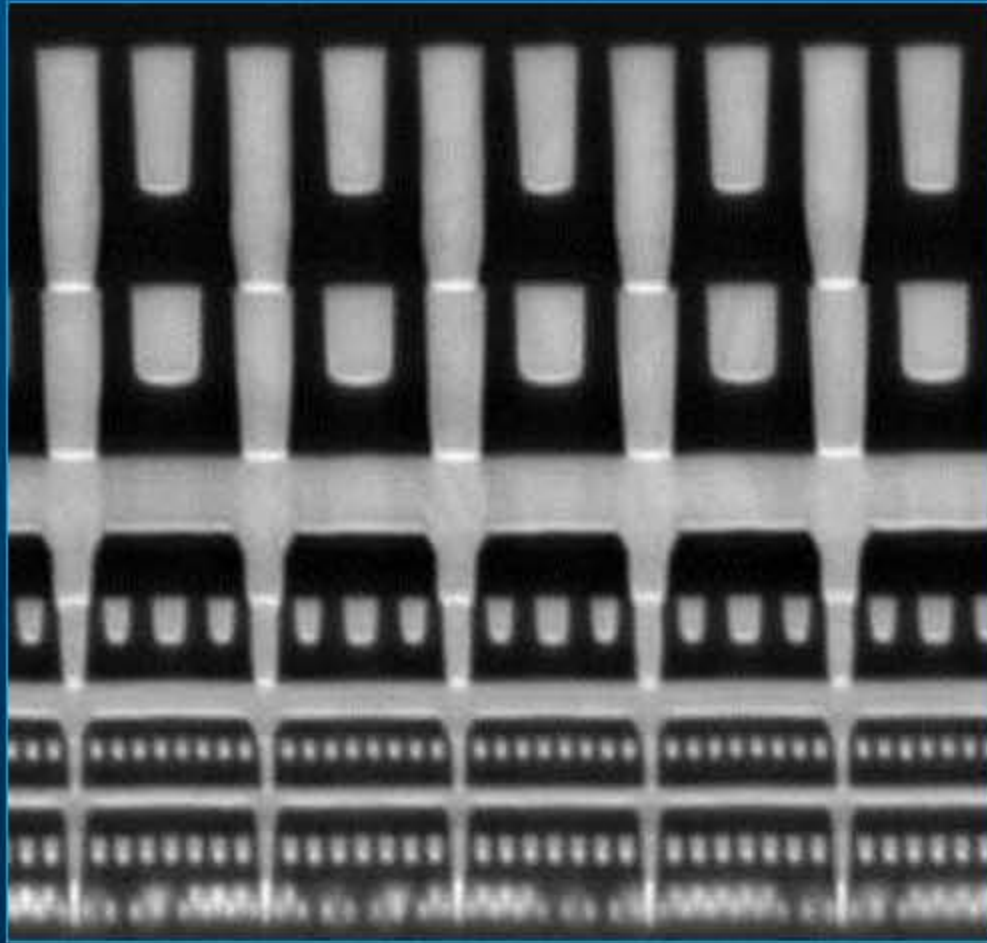


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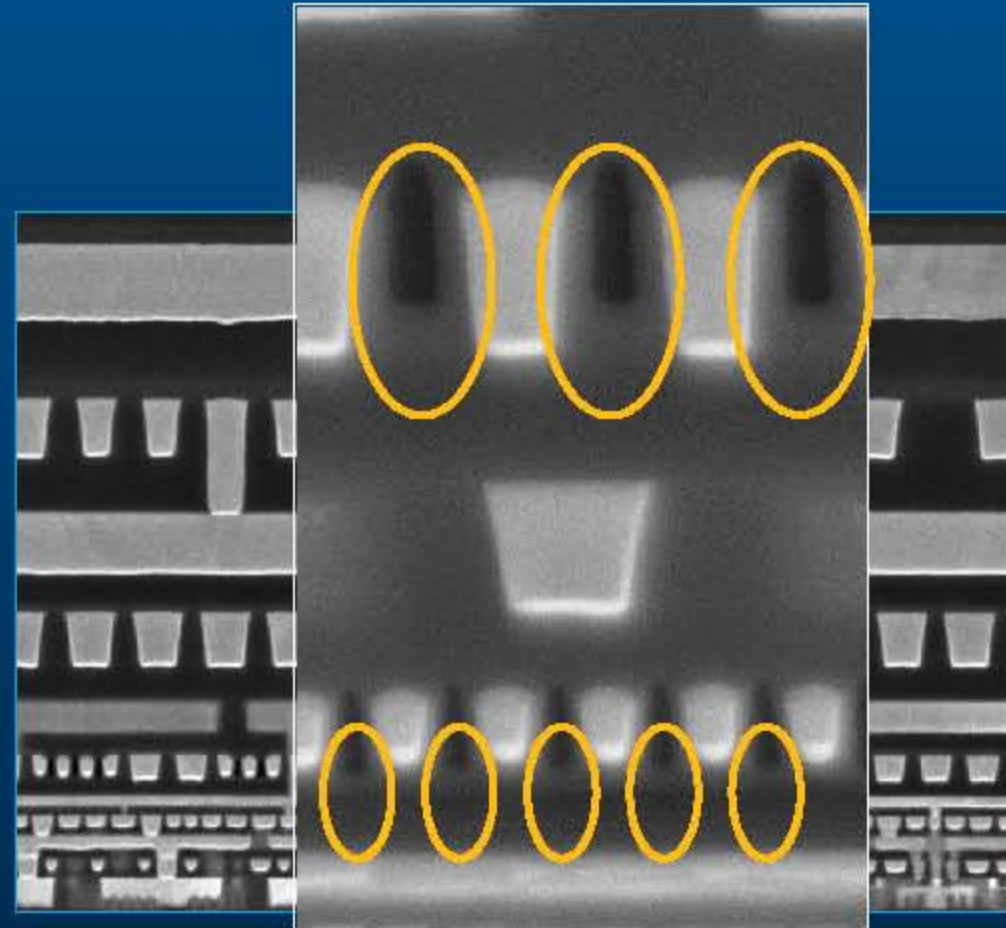
# Interconnects

22 nm Process



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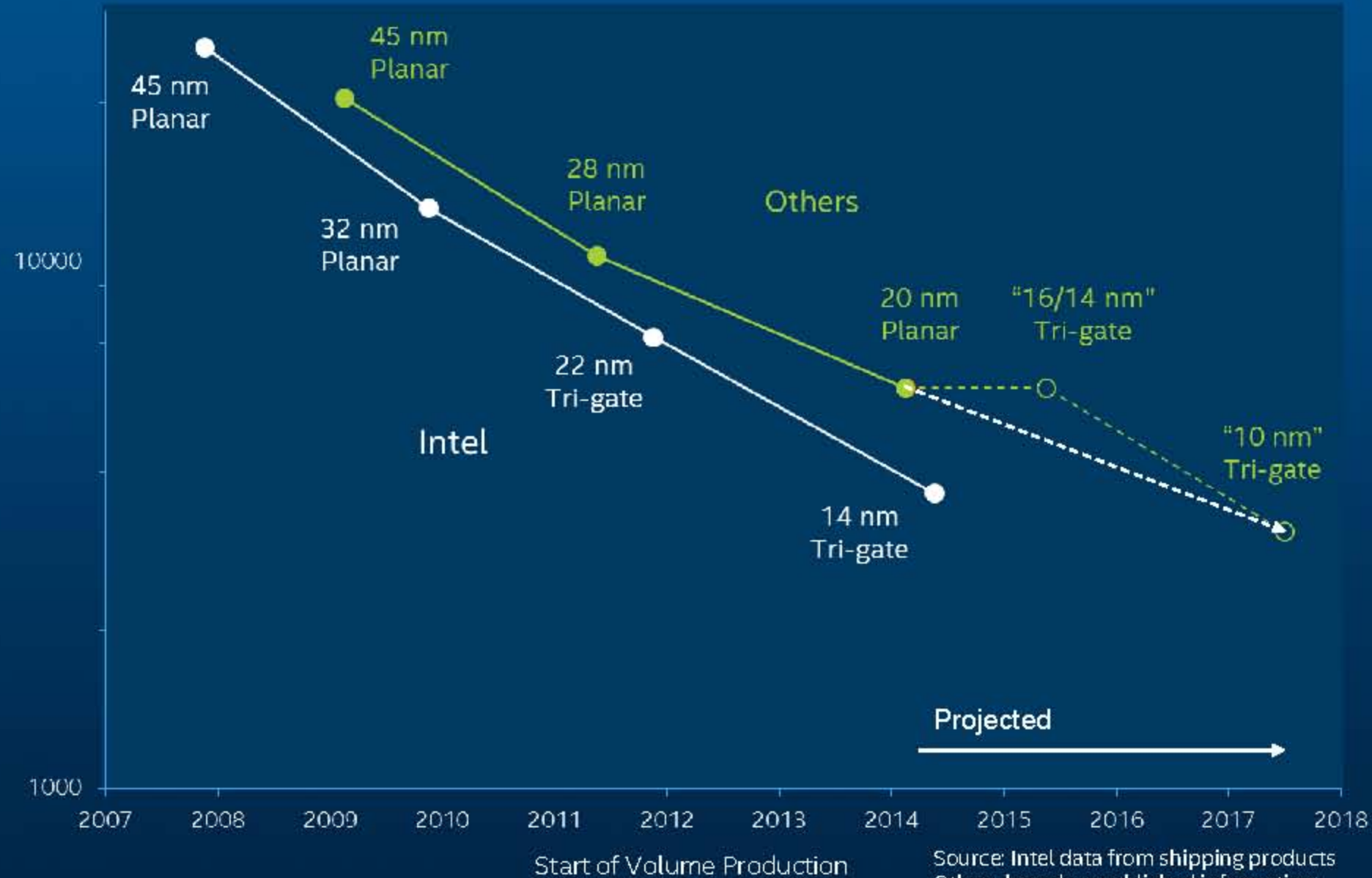
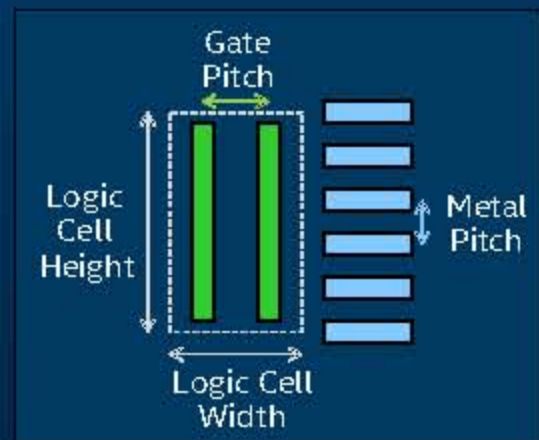
52 nm (0.65x) minimum pitch

***52 nm Interconnect Pitch Provides Better-than-normal Interconnect Scaling  
First Use of Air Gaps to Improve Interconnect Performance***



# Logic Area Scaling Trend

(Publicly available scaling information)

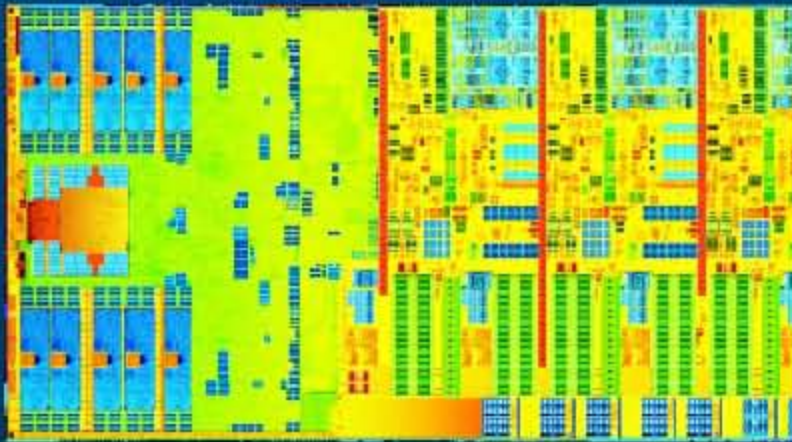


Source: Intel data from shipping products  
Others based on published information:  
45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243  
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651  
20nm: H. Shang (IBM alliance), 2012 VLSI, p. 129  
16nm: S. Wu (TSMC), 2013 IEDM, p. 224  
10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14

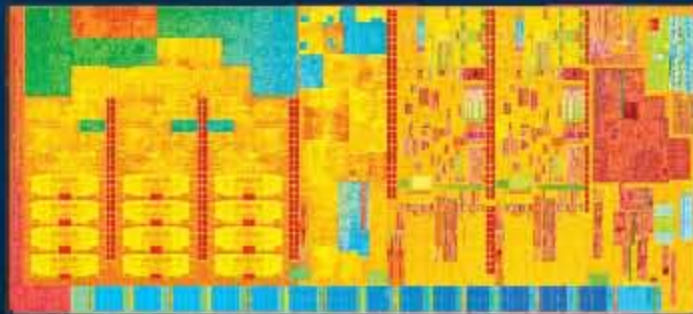


# 14nm Enables Cost and Performance Benefits

Haswell 2 X 2 (22nm)  
960M Transistors



**35%  
More  
Transistors**



**37%  
Smaller**

Broadwell 2 X 2 (14nm)  
1.3B transistors

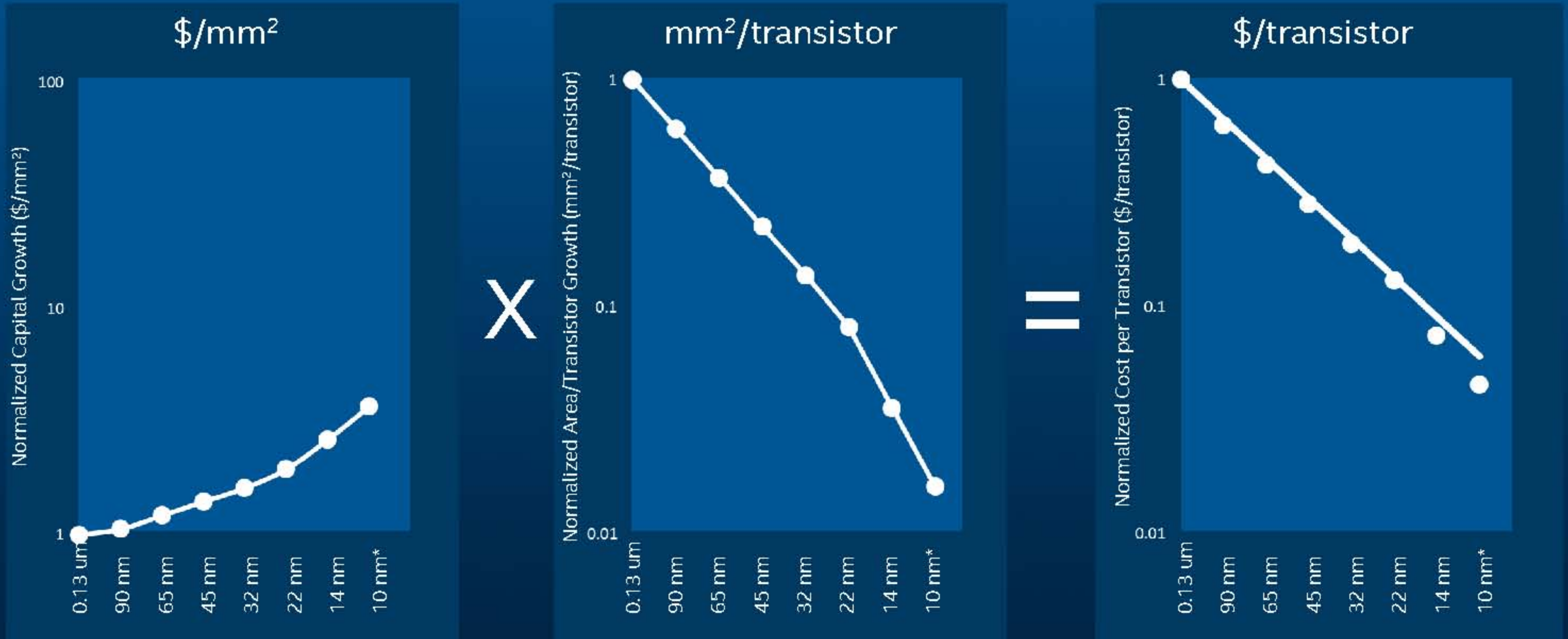
## Broadwell delivers:

- 2.2x increase in transistor density
- Up to 40% better 3D graphics perf<sup>1</sup>
- Enables <9mm fanless designs

***Industry's First 14 nm Processor in Volume Production***

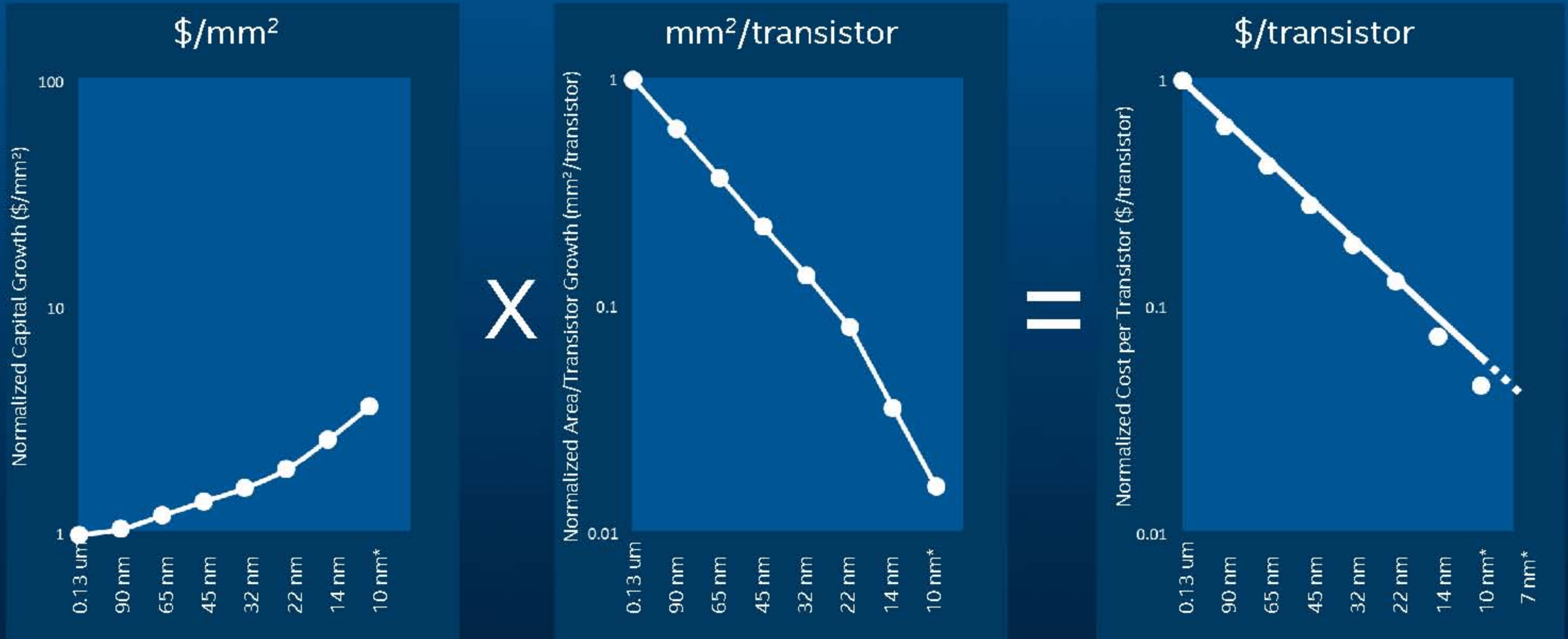
<sup>1</sup> Intel® Core™ M-5Y70 processor compared to Intel® Core™ i5-4302Y processor

# Cost Reduction On Track





# Cost Reduction On Track





# Summary

Intel Continues to Deliver Moore's Law

True Cost Reduction Remains Possible

Technology Enables Real Product Improvements

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# Risk Factors

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- The declaration and rate of dividend payments and the amount and timing of Intel’s stock buyback program are at the discretion of Intel’s board of directors, and plans for future dividends and stock buy backs and could be affected by changes in Intel’s priorities for the use of cash, such as operational spending, capital spending, acquisitions, and because of changes to Intel’s cash flows and changes in tax laws.
- Intel’s expected tax rate is based on current tax law and current expected income and may be affected by the jurisdictions in which profits are determined to be earned and taxed; changes in the estimates of credits, benefits and deductions; the resolution of issues arising from tax audits with various authorities, including payment of interest and penalties; and the ability to realize deferred tax assets.
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- Intel’s results could be affected by the timing of closing of acquisitions, divestitures and other significant transactions.
- Intel’s results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust, disclosure and other issues. An unfavorable ruling could include monetary damages or an injunction prohibiting Intel from manufacturing or selling one or more products, precluding particular business practices, impacting Intel’s ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property.

A detailed discussion of these and other factors that could affect Intel’s results is included in Intel’s SEC filings, including the company’s most recent Form 10-Q, Form 10-K and earnings release.



# Configuration Information

- Intel® Core™ M-5Y70 Processor (up to 2.60GHz, 4T/2C, 4M Cache) On Intel Reference Platform. BIOS: v80.1 Graphics: Intel® HD Graphics (driver v. 15.36.3650) Memory: 4 GB (2x2GB) Dual Channel LPDDR3-1600 SDD: Intel® 160GB OS: Windows\* 8.1 Update RTM
- Prior generation: Intel® Core™ i5-4302Y (up to 2.30GHz, 4T/2C, 3M Cache) on Intel Reference Platform. 4.5W Thermal Design Power. BIOS: WTM 137 Graphics : Intel® HD Graphics (driver v. 15.36.3650) Memory: 4 GB (2x2GB) Dual Channel LPDDR3-1600 SDD: Intel® 160GB OS: Windows\* 8.1 Update RTM. System Power Management Policy: Balance Wireless: On and connected. Battery size assumption: 35WHr.



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SANTA CLARA NOVEMBER 20