UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 8-K

CURRENT REPORT
Pursuant to Section 13 or 15(d) of
the Securities Exchange Act of 1934

Date of Report (Date of earliest event reported): July 26, 2021

INTEL CORPORATION
(Exact name of registrant as specified in its charter)

Delaware	000-06217	94-1672743
(State or Other Jurisdiction of Incorporation)	(Commission File Number)	(IRS Employer Identification No.)

2200 Mission College Blvd., Santa Clara, California	95054-1549
(Address of principal executive offices)	(Zip Code)

Registrant's telephone number, including area code: (408) 765-8080

Not Applicable
(Former name or former address, if changed since last report.)

Check the appropriate box below if the Form 8-K filing is intended to simultaneously satisfy the filing obligation of the registrant under any of the following provisions:

☐ Written communications pursuant to Rule 425 under the Securities Act (17 CFR 230.425)

☐ Soliciting material pursuant to Rule 14a-12 under the Exchange Act (17 CFR 240.14a-12)

☐ Pre-commencement communications pursuant to Rule 14d-2(b) under the Exchange Act (17 CFR 240.14d-2(b))

☐ Pre-commencement communications pursuant to Rule 13e-4(c) under the Exchange Act (17 CFR 240.13e-4(c))

Securities registered pursuant to Section 12(b) of the Act:

Title of each class	Trading Symbol(s)	Name of each exchange on which registered
Common stock, $0.001 par value	**INTC**	**Nasdaq Global Select Market**

Indicate by check mark whether the registrant is an emerging growth company as defined in Rule 405 of the Securities Act of 1933 (§230.405 of this chapter) or Rule 12b-2 of the Securities Exchange Act of 1934 (§240.12b-2 of this chapter).

Emerging growth company ☐

If an emerging growth company, indicate by check mark if the registrant has elected not to use the extended transition period for complying with any new or revised financial accounting standards provided pursuant to Section 13(a) of the Exchange Act. ☐

Item 7.01 Regulation FD Disclosure.

On July 26, 2021, Intel Corporation ("Intel") issued a press release providing an update on its manufacturing process and packaging technology roadmaps. As part of the update, Intel also introduced a new naming structure for its manufacturing process nodes, which includes the name changes summarized below:

Previous Process Node Name	New Process Node Name
10nm SuperFin	10nm SuperFin (unchanged)
10nm Enhanced SuperFin	Intel 7
Intel 7nm	Intel 4

Intel introduced additional future nodes, including Intel 3 and Intel 20A, and discussed future process and packaging technologies, such as its PowerVia, RibbonFET, Foveros Omni, and Foveros Direct technologies, in the update.

The press release is furnished as Exhibit 99.1 to this report. Intel's webcast discussing the update will be available for replay at www.intc.com.

Forward-Looking Statements

This report and the exhibit attached hereto contain forward-looking statements relating to Intel's future plans and expectations, including with respect to Intel's process and packaging technology roadmaps and schedules; innovation cadence; future technology and products and the expected benefits and availability of such technology and products, including PowerVia, RibbonFET, Foveros Omni, and Foveros Direct technologies, future process nodes, and other technologies and products; technology parity and leadership; future use, benefits, and availability of EUV and other manufacturing tools; expectations regarding suppliers, partners, and customers; Intel's strategy; manufacturing plans; manufacturing expansion and investment plans; and plans and goals related to Intel's foundry business. Such statements involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "continues," "may," "will," "would," "should," "could," "strategy," "progress," "accelerate," "path," "on-track," "roadmap," "pipeline," "cadence," "momentum," "positioned," "committed," and "deliver" and variations of such words and similar expressions are intended to identify forward-looking statements. Statements that refer to or are based on estimates, forecasts, projections, and uncertain events or assumptions also identify forward-looking statements. Such statements are based on management's current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations include, among others, Intel's failure to realize the anticipated benefits of its strategy and plans; changes in plans due to business, economic, or other factors; actions taken by competitors, including changes in competitor technology roadmaps; changes impacting our projections regarding our technology or competing technology; delays in development or implementation of our future manufacturing technologies or failures to realize the anticipated benefits of such technologies, including expected improvements in performance and other factors; delays or changes in the design or introduction of future products; changes in customer needs or plans; changes in technology trends; our ability to rapidly respond to technological developments; delays, changes in plans, or other disruptions involving manufacturing tool and other suppliers; and other factors set forth in Intel's reports filed or furnished with the Securities and Exchange Commission ("SEC"), including Intel's most recent reports on Form 10-K and Form 10-Q, available at Intel's investor relations website at www.intc.com and the SEC's website at www.sec.gov. Intel does not undertake, and expressly disclaims any duty, to update any statement made in this report and the exhibit attached hereto, whether as a result of new information, new developments or otherwise, except to the extent that disclosure may be required by law.

The information in Item 7.01 of this report and the exhibit attached hereto are furnished and shall not be treated as filed for purposes of the Securities Exchange Act of 1934, as amended.

Item 9.01 Financial Statements and Exhibits.

(d) Exhibits.

The following exhibits are provided as part of this report:

Exhibit	Description
99.1	Press release titled “Intel Accelerates Process and Packaging Innovations,” issued by Intel on July 26, 2021
104	Cover Page Interactive Data File, formatted in Inline XBRL and included as Exhibit 101

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the Registrant has duly caused this report to be signed on its behalf by the undersigned hereunto duly authorized.

INTEL CORPORATION
(Registrant)

Date: July 26, 2021

/s/ Susie Giordano
Susie Giordano
Corporate Vice President and Corporate Secretary

Intel Corporation
2200 Mission College Blvd.
Santa Clara, CA 95054-1549

News Release

Intel Accelerates Process and Packaging Innovations

Annual cadence of innovations drives leadership from silicon to system.

NEWS HIGHLIGHTS

- Roadmap of process and packaging innovations to power next wave of products through 2025 and beyond
- Two breakthrough process technologies: RibbonFET, Intel's first new transistor architecture in more than a decade, and PowerVia, an industry-first for backside power delivery
- Continued leadership in advanced 3D packaging innovations with Foveros Omni and Foveros Direct
- New node naming to create consistent framework, more accurate view of process nodes for customers and the industry as Intel enters the angstrom era of semiconductors
- Strong momentum for Intel Foundry Services (IFS) with first customer announcements

SANTA CLARA, Calif., July 26, 2021 – Intel Corporation today revealed one of the most detailed process and packaging technology roadmaps the company has ever provided, showcasing a series of foundational innovations that will power products through 2025 and beyond. In addition to announcing RibbonFET, its first new transistor architecture in more than a decade, and PowerVia, an industry-first new backside power delivery method, the company highlighted its planned swift adoption of next-generation extreme ultraviolet lithography (EUV), referred to as High Numerical Aperture (High NA) EUV. Intel is positioned to receive the first High NA EUV production tool in the industry.

"Building on Intel's unquestioned leadership in advanced packaging, we are accelerating our innovation roadmap to ensure we are on a clear path to process performance leadership by 2025," Intel CEO Pat Gelsinger said during the global "Intel Accelerated"[1] webcast. "We are leveraging our unparalleled pipeline of innovation to deliver technology advances from the transistor up to the system level. Until the periodic table is exhausted, we will be relentless in our pursuit of Moore's Law and our path to innovate with the magic of silicon."

The industry has long recognized that traditional nanometer-based process node naming stopped matching the actual gate-length metric in 1997. Today, Intel introduced a new naming structure for its process nodes, creating a clear and consistent framework to give customers a more accurate view of process nodes across the industry. This clarity is more important than ever with the launch of Intel Foundry Services. "The innovations unveiled today will not only enable Intel's product roadmap; they will also be critical for our foundry customers," Gelsinger said. "The interest in IFS has been strong and I'm thrilled that today we announced our first two major customers. IFS is off to the races!"

1 https://www.intel.com/content/www/us/en/newsroom/resources/press-kit-accelerated-event-2021.html

— more —

Intel technologists described the following roadmap with the new node names and the innovations enabling each node[2]:

- **Intel 7** delivers an approximately 10% to 15% performance-per-watt increase versus Intel 10nm SuperFin, based on FinFET transistor optimizations. Intel 7 will be featured in products such as Alder Lake for client in 2021 and Sapphire Rapids for the data center, which is expected to be in production in the first quarter of 2022.
- **Intel 4** fully embraces EUV lithography to print incredibly small features using ultra-short wavelength light. With an approximately 20% performance-per-watt increase, along with area improvements, Intel 4 will be ready for production in the second half of 2022 for products shipping in 2023, including Meteor Lake for client and Granite Rapids for the data center.
- **Intel 3** leverages further FinFET optimizations and increased EUV to deliver an approximately 18% performance-per-watt increase over Intel 4, along with additional area improvements. Intel 3 will be ready to begin manufacturing products in the second half of 2023.
- **Intel 20A** ushers in the angstrom era with two breakthrough technologies, RibbonFET and PowerVia. RibbonFET, Intel's implementation of a gate-all-around transistor, will be the company's first new transistor architecture since it pioneered FinFET in 2011. The technology delivers faster transistor switching speeds while achieving the same drive current as multiple fins in a smaller footprint. PowerVia is Intel's unique industry-first implementation of backside power delivery, optimizing signal transmission by eliminating the need for power routing on the front side of the wafer. Intel 20A is expected to ramp in 2024. The company is also excited about the opportunity to partner with Qualcomm using its Intel 20A process technology.
- **2025 and Beyond:** Beyond Intel 20A, Intel 18A is already in development for early 2025 with refinements to RibbonFET that will deliver another major jump in transistor performance. Intel is also working to define, build and deploy next-generation High NA EUV, and expects to receive the first production tool in the industry. Intel is partnering closely with ASML to assure the success of this industry breakthrough beyond the current generation of EUV.

"Intel has a long history of foundational process innovations that have propelled the industry forward by leaps and bounds," said Dr. Ann Kelleher, senior vice president and general manager of Technology Development. "We led the transition to strained silicon at 90nm, to high-k metal gates at 45nm and to FinFET at 22nm. Intel 20A will be another watershed moment in process technology with two groundbreaking innovations: RibbonFET and PowerVia."

With Intel's new IDM 2.0 strategy, packaging is becoming even more important to realizing the benefits of Moore's Law. Intel announced that AWS will be the first customer to use IFS packaging solutions, while also providing the following insights into the company's industry-leading advanced packaging roadmap:

- **EMIB** continues to lead the industry as the first 2.5D embedded bridge solution, with products shipping since 2017. Sapphire Rapids will be the first Intel® Xeon® data center product to ship

2 http://www.intel.com/processinnovation

in volume with EMIB (embedded multi-die interconnect bridge). It will also be the first dual-reticle-sized device in the industry, delivering nearly the same performance as a monolithic design. Beyond Sapphire Rapids, the next generation of EMIB will move from a 55-micron bump pitch to 45 microns.

- **Foveros** leverages wafer-level packaging capabilities to provide a first-of-its-kind 3D stacking solution. Meteor Lake will be the second-generation implementation of Foveros in a client product and features a bump pitch of 36 microns, tiles spanning multiple technology nodes and a thermal design power range from 5 to 125W.
- **Foveros Omni** ushers in the next generation of Foveros technology by providing unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs. Foveros Omni allows die disaggregation, mixing multiple top die tiles with multiple base tiles across mixed fab nodes and is expected to be ready for volume manufacturing in 2023.
- **Foveros Direct** moves to direct copper-to-copper bonding for low-resistance interconnects and blurs the boundary between where the wafer ends and where the package begins. Foveros Direct enables sub-10-micron bump pitches providing an order of magnitude increase in the interconnect density for 3D stacking, opening new concepts for functional die partitioning that were previously unachievable. Foveros Direct is complementary to Foveros Omni and is also expected to be ready in 2023.

The breakthroughs discussed today were primarily developed at Intel's facilities in Oregon and Arizona, cementing the company's role as the only leading-edge player with both research and development and manufacturing in the U.S. Additionally, the innovations draw on close collaboration with an ecosystem of partners in both the U.S. and Europe. Deep partnerships are key to bringing foundational innovations from the lab to high-volume manufacturing, and Intel is committed to partnering with governments to strengthen supply chains and drive economic and national security.

The company closed its webcast by confirming more details on its Intel InnovatiON event. Intel InnovatiON will be held in San Francisco and online on Oct. 27-28, 2021. More information is available at the Intel ON website[3].

For more information on Intel's process roadmap and node naming, visit the process factsheet[4]. To watch a replay of today's webcast, visit the Intel Newsroom[5] or Intel's investor relations website[6].

About Intel

Intel (Nasdaq: INTC) is an industry leader, creating world-changing technology that enables global progress and enriches lives. Inspired by Moore's Law, we continuously work to advance the design and manufacturing of semiconductors to help address our customers' greatest challenges. By embedding intelligence in the cloud, network, edge and every kind of computing device, we unleash the potential of data to transform business and society for the better. To learn more about Intel's innovations, go to newsroom.intel.com and intel.com.

3 https://www.intel.com/content/www/us/en/events/on-event-series.html.
4 http://www.intel.com/processinnovation
5 https://newsroom.intel.com/
6 http://www.intc.com/

Forward-Looking Statements

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All product and service plans, roadmaps, and performance figures are subject to change without notice. Process performance parity and leadership expectations are based on performance-per-watt projections. Future node performance and other metrics, including power and density, are projections and are inherently uncertain.

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